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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,805	03/26/2004	GENG-LIN CHEN	12264-US-PA	2804
31561	7590	03/06/2006	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100 TAIWAN			STIGLIC, RYAN M	
			ART UNIT	PAPER NUMBER
			2112	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/708,805		CHEN ET AL.	
	Examiner		Art Unit	
	Ryan M. Stiglic		2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

1. Claims 1-15 are pending and have been examined.
2. Claims 1-15 are rejected.

Claim Objections

3. Claim 7 is objected to because of the following informalities: Claim 7 recites, "...temptempa bus arbitrator..." which the Examiner believes is a typographical mistake and will treat the claims as meaning "...a bus arbitrator..." for the remainder of the Office Action. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 12 recites the limitation "the first device" and "the second device" in lines 7-12 of page 4 of the claims. There is insufficient antecedent basis for this limitation in the claim. For the sake of advanced prosecution the Examiner will interpret "a memory unit" as the first device and "a memory card compatible device" as the second device.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Lendaro (US 20040036808A1).

For claim 1 Lendaro discloses:

A system for accessing a plurality of devices using a single bus, comprising:

- a first device (Fig. 3, items 44, 46 and 48);
- a second device (Fig. 3, items 52, 54, 56 and 58);
- a shared bus, coupled to the first device (Fig. 3, shown as “Clock” and “Data” lines leaving “Main Micro” 42);
- a bus isolator, coupled to the shared bus and the second bus for isolating the second device from the shared bus or connecting the second device to the shared bus (Fig. 3, item 36; paragraphs [0030-0031]); and
- a control apparatus (Fig. 3, item 42) coupled to the shared bus so that the bus isolator isolates the second device from the shared bus when the control apparatus needs to access

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the first device and the bus isolator connects the second device with the shared bus when the control apparatus needs to access the second device (paragraphs [0009, 0038, 0042]).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 2-3 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lendaro (US 20040036808A1) in view of Matsuoka (US006009492A).

Lendaro discloses a system and method for isolating a second device from a shared bus when a control apparatus needs to access a first device and a bus isolator connects the second device with the shared bus when the control apparatus needs to access the second device. Lendaro however, fails to teach a bus exchanger and bus arbitrator within the control apparatus for connecting the shared bus with circuitry internal to the control apparatus according to the device the control apparatus wishes to communicate with.

Matsuoka teaches an expansion system "...which can realize reductions in size and cost by decreasing the numbers of input/output pins and the numbers of connectors of controllers for interfacing between various expansion devices and a computer body (col. 1, ll. 55-59)."

Matsuoka teaches a control apparatus (Fig. 1 and 2, item 3) that reduces the number of buses and

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pins required to connect a plurality peripherals by realizing a bus exchanger/switch (Fig. 2, items 20A and 20B) that "...switches the bus signal lines for connecting the input/output section 21 connected to the expansion connector 8 to the respective controllers 22 to 24...(col. 7, ll. 25-28)" under the control of the bus arbitrator (I/O controller 3 as a whole serves as the bus arbitrator since "The I/O controller 3 switches the bus signal lines for connecting the input/output section 21 connected to the expansion connector 8 to the respective controllers 22 to 24 through the bus switching circuits 20A and 20B (col. 7, ll. 25-28).")

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the I/O controller of Matsuoka as the "Main Micro" of Lendaro such that reductions in size and cost by decreasing the numbers of input/output pins and the numbers of connectors of controllers for interfacing between various expansion devices is achieved.

For claim 2 Lendaro in view of Matsuoka teach:

The system of claim 1, wherein the control apparatus further comprises:

- a bus exchanger, coupled to the shared bus for switching the authority for the shared bus between different devices (Matsuoka; Fig. 3, items 20A and 20B; col. 5, line 66 – col. 6, line 7; col. 7, ll. 25-28); and
- a bus arbitrator, coupled to the bus exchanger so that the bus arbitrator controls the bus exchanger to connect the shared bus with a circuit internally linked to the first device when the control apparatus needs to access the first device and the bus arbitrator controls the bus exchanger to connect the shared bus with a circuit internally linked to the second

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device when the control apparatus needs to access the second device (Matsuoka; col. 7, ll. 25-28).

For claims 3 and 8 Lendaro in view of Matsuoka teach:

The system of claim 2, wherein a pre-defined isolation period must pass before the bus exchanger is permitted to switch the device for authority for the shared bus (Lendaro; paragraph [0042]).

For claim 7 Lendaro in view of Matsuoka teach:

A control apparatus (Lendaro; Fig. 3, 42; Matsuoka; Fig. 1 and 2, item 3) for accessing a plurality of devices (Lendaro; Fig. 3, items 44, 46, 48, 52, 54, 56 and 58; Matsuoka; Fig. 1, items 10 and 11) through a single bus (Lendaro; Fig. 3, shown as “Clock” and “Data” lines leaving “Main Micro” 42; Matsuoka; shown as the arrowed lines between “expansion connector” 8 and connectors 10A and 11A, 11B), the control apparatus connects to a first device through a shared bus and the control apparatus also connects to a second device through the shared bus and a bus isolator (Lendaro; Fig. 3, item 36) (Lendaro; paragraphs [0009, 0030-0031, 0038, 0042];

Matsuoka; col. 7, ll. 25-28), the control apparatus comprising :

- a bus exchanger, coupled to the shared bus for switching the authority of device for the shared bus (Matsuoka; Fig. 3, items 20A and 20B; col. 5, line 66 – col. 6, line 7; col. 7, ll. 25-28); and
- a bus arbitrator coupled to the bus exchanger such that the bus arbitrator controls the bus exchanger to connect with a circuit internally linked to the first device and to activate the

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bus isolator to isolate the second device from the shared bus when the control apparatus needs to access the first device and the bus arbitrator controls the bus exchanger to connect with a circuit internally linked related to the second device when the control apparatus needs to access the first device (Matsuoka; col. 7, ll. 25-28).

10. Claims 4-6 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lendaro (US 20040036808A1) in view of Matsuoka (US006009492A) as applied to claims 1, 2 and 7 above and further in view of what was commonly known in the art at the time of applicant's invention as evidenced by Bender et al. (US. 5,519,851).

For claims 4 and 9 Lendaro in view of Matsuoka teach:

Matsuoka teaches one type of peripheral attached to the expansion connector 8 is a PC Card type device. The I/O controller 3 of Matsuoka includes a PC Card Controller (Fig. 2, 22) that is associated with a connected PC Card (Fig. 1, 10) when the I/O controller wishes to communicate with the PC Card (col. 7, ll. 25-28). The PC card slot is an expansion slot for PC cards, which is based on the standards of PMCIA (Personal Computer Memory Card International Association) (col. 1, ll. 14-17). The teachings of Matsuoka therefore suggest using a PC Card device, as either a first or second device of Lendaro would have been obvious because it can be implemented with the serial bus of Lendaro using the I/O controller 3. Furthermore, *Official Notice* is taken that "...a wide variety of external peripheral and memory devices (may be) implemented in the PC card format..." as evidenced by Bender (col. 1, line 60 – col. 2, line 6).

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For claims 5 and 10 Lendaro in view of Matsuoka teach:

The system of claim 4, wherein the memory card compatible device is either a memory card (see *Official Notice* and Bender et al. col. 1, line 60 – col. 2, line 6) or a card reader.

For claims 6 and 11 Lendaro in view of Matsuoka teach:

Matsuoka teaches one type of peripheral attached to the expansion connector 8 is a PC Card type device. The I/O controller 3 of Matsuoka includes a PC Card Controller (Fig. 2, 22) that is associated with a connected PC Card (Fig. 1, 10) when the I/O controller wishes to communicate with the PC Card (col. 7, ll. 25-28). The PC card slot is an expansion slot for PC cards, which is based on the standards of PMCIA (Personal Computer Memory Card International Association) (col. 1, ll. 14-17). The teachings of Matsuoka therefore suggest using a PC Card device, as either a first or second device of Lendaro would have been obvious because it can be implemented with the serial bus of Lendaro using the I/O controller 3. Furthermore, *Official Notice* is taken that “...a wide variety of external peripheral and memory devices (may be) implemented in the PC card format...” as evidenced by Bender (col. 1, line 60 – col. 2, line 6).

Lendaro also teaches that one type of integrated circuit connected to the serial bus is a memory (Fig. 3, 58; [0035-0036]). Although shown as a second device, one of ordinary skill in the art would realize that Memory 58 merely represents a type integrated circuit and as such a memory device could easily be used as “Other I²C devices” 44, 46 or 48.

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For claim 12 Lendaro in view of Matsuoka teach:

A system for accessing a plurality of devices through a single bus, comprising:

- a memory unit (*please see the rejection of claims 6 and 11 above*);
- a memory card compatible device (*please see the rejection of claims 4-5 and 9-10 above*);
- a shared bus (Lendaro; Fig. 3, shown as “Clock” and “Data” lines leaving “Main Micro” 42; Matsuoka; shown as the arrowed lines between “expansion connector” 8 and connectors 10A and 11A, 11B), coupled to the memory unit; and
- a control apparatus coupled to the shared bus such that the control apparatus controls the shared bus to connect with a circuit internally linked to the first device when the control apparatus needs to access the first device and the control apparatus controls the shared bus to connect with a circuit internally linked to the second device when the control apparatus needs to access the second device (Matsuoka; col. 7, ll. 25-28).

For claim 13 Lendaro in view of Matsuoka teach:

The system of claim 12, wherein a pre-defined isolation period must pass before the bus exchanger is permitted to switch the device for authority for the shared bus (Lendaro; paragraph [0042]).

For claim 14 Lendaro in view of Matsuoka teach:

Matsuoka teaches one type of peripheral attached to the expansion connector 8 is a PC Card type device. The I/O controller 3 of Matsuoka includes a PC Card Controller (Fig. 2, 22) that is

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associated with a connected PC Card (Fig. 1, 10) when the I/O controller wishes to communicate with the PC Card (col. 7, ll. 25-28). The PC card slot is an expansion slot for PC cards, which is based on the standards of PMCIA (Personal Computer Memory Card International Association) (col. 1, ll. 14-17). The teachings of Matsuoka therefore suggest using a PC Card device as either a first or second device of Lendaro would have been obvious because it can be implemented with the serial bus of Lendaro using the I/O controller 3. Furthermore, *Official Notice*, is taken that “...a wide variety of external peripheral and memory devices (may be) implemented in the PC card format...” as evidenced by Bender (col. 1, line 60 – col. 2, line 6).

For claim 15 Lendaro in view of Matsuoka teach:

Matsuoka teaches one type of peripheral attached to the expansion connector 8 is a PC Card type device. The I/O controller 3 of Matsuoka includes a PC Card Controller (Fig. 2, 22) that is associated with a connected PC Card (Fig. 1, 10) when the I/O controller wishes to communicate with the PC Card (col. 7, ll. 25-28). The PC card slot is an expansion slot for PC cards, which is based on the standards of PMCIA (Personal Computer Memory Card International Association) (col. 1, ll. 14-17). The teachings of Matsuoka therefore suggest using a PC Card device as either a first or second device of Lendaro would have been obvious because it can be implemented with the serial bus of Lendaro using the I/O controller 3. Furthermore, *Official Notice*, is taken that “...a wide variety of external peripheral and memory devices (may be) implemented in the PC card format...” as evidenced by Bender (col. 1, line 60 – col. 2, line 6).

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Lendaro also teaches that one type of integrated circuit connected to the serial bus is a memory (Fig. 3, 58; [0035-0036]). Although shown as a second device, one of ordinary skill in the art would realize that Memory 58 (EEPROM “read-only memory”) merely represents a type integrated circuit and as such a memory device could easily be used as “Other I²C devices” 44, 46 or 48.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure because it pertains to sharing a bus connection between host controllers and isolation of devices using switches.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RMS



PAUL R. MYERS
PRIMARY EXAMINER